David A. Papa

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Vital Statistics
Date of Birth: February 03, 1981
Place of Birth: Royal Oak, Michigan, USA

Education

University of Michigan Ann Arbor **Grad Date:** May 2007
Degree: Bachelor of Computer Engineering **GPA:** 3.6/4.0
Magna Cum Laude
Degree: Masters of Computer Science in Engineering **GPA:** 7.25/9.0
Currently: Ph. D. Candidate in Computer Science in Engineering

- **VLSICAD**
- Logic Design, Synth., and Verif.
- Adv. Compiler Construction
- Operating Systems
- Adv. Computer Architecture
- Linear Algebra
- Adv. Electrical Engineering
- Theory of Calculus
- Data Structures and Algorithms
- Adv. OO Programming Concepts
- Software Engineering
- Adv. Algorithm Analysis
- Embedded System Design
- Artificial Intelligence
- Electromagnetics
- Combinatorics & Graph Theory

Computer Skills

Languages: C/C++, Tcl and Perl (familiarity with several others).
Libraries: Standard C++ Library, Qt, OpenGL, and OpenAccess.
Environments: Linux, Windows, AIX, Solaris.
Applications: g++, svn, cvs, MS Devel. Studio, gdb, gprof, valgrind.

Experience

IBM Austin, TX
Research Intern May 2006-Present
- Austin Research Lab (ARL)
- Focus on improvements to **Placement Driven Synthesis (PDS)**

University of Michigan Ann Arbor, MI
Graduate Student Research Assistant September 2002-May 2006
- Advanced Computer Architecture Lab.
- Primary focus on EDA Tools for VLSICAD.
- Strong experience with **Capo**, a leading academic placement tool.

Cadence Berkeley Labs Berkeley, CA
Research Scientist June 2004-September 2004
- Ongoing developer of open-source software for Open Access 2.2.
- Designer of programmer's tool-kit **OAGear** including placer and GUI.

University of Michigan Ann Arbor, MI
Software Engineer/Research Scientist May 2001 - September 2001
- Research in the field of VLSICAD.
- Programmer of new algorithms relevant to the field.

Honors

Early Tenure Inventor – IBM	2008
First Plateau Invention Achievement Award – IBM	2007
Best Contribution Award – IWLS Programming Competition http://www.eetimes.com/news/latest/showArticle.jhtml?articleID=188702906	2006
Eta Kappa Nu engineering honor society	2001
Class Honors	2000
University Honors	2000
University of Michigan Dean's List	1999, 2000, 2001
Cranbrook Kingswood Prize Program Award	1996, 1997, 1998, 1999

Patents

Filed

- C. J. Alpert, A. K. Karandikar, Z. Li, G.-J. Nam, D. A. Papa and C. N. Sze, "Method for Incremental, Timing-driven, Physical-synthesis Optimization," September 2007
- C. J. Alpert, Z. Li, M. D. Moffitt and D. A. Papa "Method for Incremental, Timing-driven, Physical-synthesis Discrete Optimization," November 2007
- C. J. Alpert, Z. Li, T. Luo, D. A. Papa and C. N. Sze, "Improved Method for Incremental, Timing-driven, Physical-synthesis Optimization Under a Linear Delay Model," November 2007
- C. J. Alpert, Z. Li, D. A. Papa and C. N. Sze, "Methods for Optimal Timing-driven Cloning under a Linear Delay Model," November 2007
- M. D. Moffitt and D. A. Papa, "Method for Bounded Transactional Timing Analysis," June 2008

Publications

In Books

- D. A. Papa and I. L. Markov, "Hypergraph Partitioning and Clustering," in Approximation Algorithms and Metaheuristics, T. Gonzalez, ed.; CRC Press, 2007, in print.
- J. A. Roy, D. A. Papa and I. L. Markov, "Capo: Congestion-aware Placement for Standard-cell and RTL Netlists with Incremental Capability," in Modern Circuit Placement: Best Practices and Results, G.-J. Nam and J. Cong, eds; Springer, 2007.

In Journals

- D. A. Papa, T. Luo, M. D. Moffitt, C. N. Sze, Z. Li, G.-J. Nam, C. J. Alpert and I. L. Markov, "RUMBLE: An Incremental, Timing-driven, Physical-synthesis Optimization Algorithm," to appear in IEEE Trans. on Computer-Aided Design, 2009.
- J. A. Roy, D. A. Papa and I. L. Markov, "Fine Control of Local Whitespace in Placement," to appear in VLSI Design, 2009.
- K.-H. Chang, D. A. Papa, I. L. Markov, V. Bertacco, "InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization," to appear in IEEE Design and Test of Computers, 2008.
- J. A. Roy, S. N. Adya, D. A. Papa and I. L. Markov, "Min-cut Floorplacement," *IEEE Trans. on Computer Aided Design* (TCAD), 2006, to appear.

Publications

In Conferences

- Tao Luo, David A. Papa, Zhuo Li, Cliff C. N. Sze, Charles J. Alpert and David Z. Pan, “Pyramids: An Efficient Computational Geometry-based Approach for Timing-driven Placement,” to Appear in Proc. International Conference on Computer Aided Design (ICCAD) 2008. (best paper award finalist)
- Michael D. Moffitt, David A. Papa, Zhuo Li, Charles J. Alpert “Path Smoothing via Discrete Optimization,” Design Automation Conference (DAC) pp. 724-727, Anaheim, CA, July 2008.
- D. A. Papa, T. Luo, M. D. Moffitt, C. N. Sze, Z. Li, G.-J. Nam, C. J. Alpert and I. L. Markov, “RUMBLE: An Incremental, Timing-driven, Physical-synthesis Optimization Algorithm,” Int'l Symposium on Physical Design (ISPD), pp. 2-9, Portland, Oregon, 2008.
- K.-H. Chang, D. A. Papa, I. L. Markov and V. Bertacco, “InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization,” ISQED 2007.
- J. A. Roy, D. A. Papa, A. N. Ng, I. L Markov, “Satisfying Whitespace Requirements in Top-down Placement,” Proc. Int'l Symp. on Physical Design (ISPD), pp. 206-208, San Jose, CA, April 2006.
- J. A. Roy, D. A. Papa, S. N. Adya, H. H. Chan, J. F. Lu, A. N. Ng, I. L. Markov, “Capo: Robust and Scalable Open-Source Min-cut Floorplacer,” *Intl. Symposium on Physical Design (ISPD)*, 2005, pp. 224-227.
- D. A. Papa, I. L. Markov and P. Chong, “Utility of OpenAccess in Academic Research,” Proc. Asia and South Pacific Design Automation Conference (ASPDAC), pp. 440-441, Yokohama, Japan, January 2006.
- Z. Xiu, D. Papa, P. Chong, A. Kuehlmann, R. Rutenbar, I. Markov, “Early Research Experience with OpenAccess Gear: An Open Source Development Environment for Physical Design,” *Intl. Symposium on Physical Design (ISPD)*, 2005, pp. 94-100.
- S. N. Adya, S. Chaturvedi, J. A. Roy, D. A. Papa and I. L. Markov, “Unification of Partitioning, Floorplanning and Placement,” Intl. Conf. Computer-Aided Design (ICCAD), San Jose, CA, November 2004, pp. 550-557
- D. A. Papa, S. N. Adya and I. L. Markov, “Constructive Benchmarking for Placement,” *Great Lakes Symp. on VLSI* (GLSVLSI), 2004, pp. 113-118.

Invited Talks

- D. A. Papa and I. L. Markov, “Fast Simulation and Equivalence Checking Using OpenAccess,” the Open Access conference (OA), San Jose, CA, November 2006.
- D. A. Papa, I. L. Markov and P. Chong, “Utility of OpenAccess in Academic Research,” Proc. Asia and South Pacific Design Automation Conference (ASPDAC), pp. 440-441, Yokohama, Japan, January 2006.
- J. A. Roy, D. A. Papa, J. F. Lu, A. N. Ng, I. L. Markov, “Tool Development For Multi-Million Gate Designs,” workshop on Electronic Design Processes, 2005.

In Workshops

- K.-H. Chang, D. A. Papa, I. L. Markov and V. Bertacco, “Fast Simulation and Equivalence Checking Using OAGear,” IWLS, pp. 270-271, Denver, CO, June 2006.

Reviews

Journals

- IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD).